AD9788/87/85 Evaluation Board

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Getting Started with the AD9788/87/85 Evaluation Board

WHAT'S IN THE BOX

AD978x-DPG2-EBZ Evaluation Board
Mini-USB Cable
AD9788 Evaluation Board CD

EXAMPLE EQUIPMENT LIST

+5Vdc Power Supply: Agilent E3630A
Digital Pattern Generator (DPG2): ADI HSC-DAC-DPG-BZ
DAC Clock Source: R&S SML 02
AQM LO Clock Source: R&S SMA100A
Spectrum Analyzer: Agilent PSAA or R&S FSU
PC: Windows PC with 2 or more USB ports (See Appendix for system requirements)

INTRODUCTION

The AD9788/87/85 Evaluation Boards (model AD978x-DPG2–EBZ) connect directly to the Analog Devices Digital Pattern Generator 2 (DPG2) to allow for quick evaluation of the AD9788 family of DACs. The DPG2 allows the user to create many types of digital vectors and transmit these at speed to the AD9788 in any of the DAC operating modes. The AD9788 evaluation board is configured over USB with accompanying PC software. The evaluation board includes the ADL5375 quadrature modulator and the AD9516 clock chip so the board can be configured as a transmit chain in addition to evaluating the DAC as a standalone part. The AD9516 can be used to compare the on chip PLL performance to the AD9516 clock multiplication performance in terms of jitter or phase noise.

SOFTWARE INSTALLATION

The AD9788 application software should be installed on the PC prior connecting the hardware to the PC. The DAC Software Suite is included on the Evaluation Board CD, or can be downloaded from the DPG web site at **http://www.analog.com/dpg**. This will install DPGDownloader (for loading vectors into the DPG2) and the AD9788 SPI application.

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HARDWARE SETUP (DAC OUTPUT)

Once the DPGDownloader software is installed, the hardware can be connected as shown in Figure 1. A single 5V power supply powers the evaluation board. The power supply should be able to source up to 2A to cover all of the board's operating conditions. A low jitter clock source (< 0.5ps RMS) should be used for the DACCLK. A sinusoidal clock output level of 0dBm to +4dBm is optimal. By default, the DAC outputs are connected to the filter driving the quadrature modulator so the output signal will be at the RF output of the ADL5375, J6. The modifications for observing the DAC outputs and different clocking options will be explained. The evaluation board plugs directly into the DPG2. The PC connects to both the DPG2 and the evaluation board through USB cables.

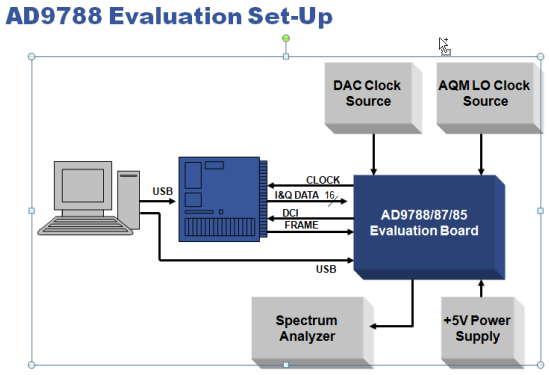


Figure 1- Bench Set-Up

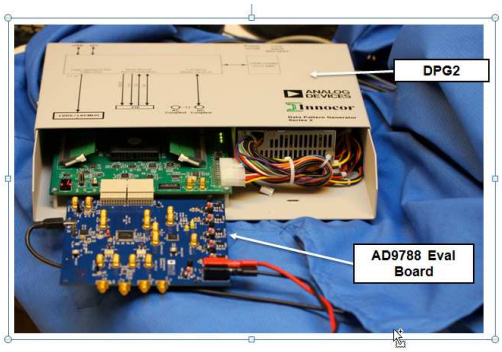


Figure 2- DPG2 and AD9788 Evaluation Board

GETTING STARTED – SINGLE TONE TEST

It is suggested that the basic set-up is verified before making any modifications to the evaluation board.

Basic Hardware Set-Up

Connect the equipment to the AD9788 evaluation board per the following table:

Equipment	**Connects to AD978x Eval Board**
Power Supply	P4 (+5V), P5 (GND)
Signal Source Clk	J2 (DAC Clock), Set source to 200MHz, 3dBm output
Signal Source LO	J19 (LO IN), Set source to desired LO (i.e. 900 or 1800 MHz, 3dBm output when using the ADL5375 to mix up to the antenna frequency.
PC USB Cable	XP2
Spectrum Analyzer	J6 (RF_OUT)
DPG2	P1 and P2

DPGDownloader Software

Power up the DPG and connect the USB cable to the PC. Next, run the DPGDownloader Software. A shortcut will be installed to your Start menu during the installation of the DAC Software Suite. To begin, click on the DPGDownloader shortcut in your Programs menu, typically at Start > Programs > Analog Devices > DPG > DPGDownloader.

The basic parts of the DPGDownloader window are: Hardware Config Panel, SPI GUI Launch Button, Vector Generation Pull-Down Menu, Vector Palette, Vector Selection Panel and the Download and Play buttons.

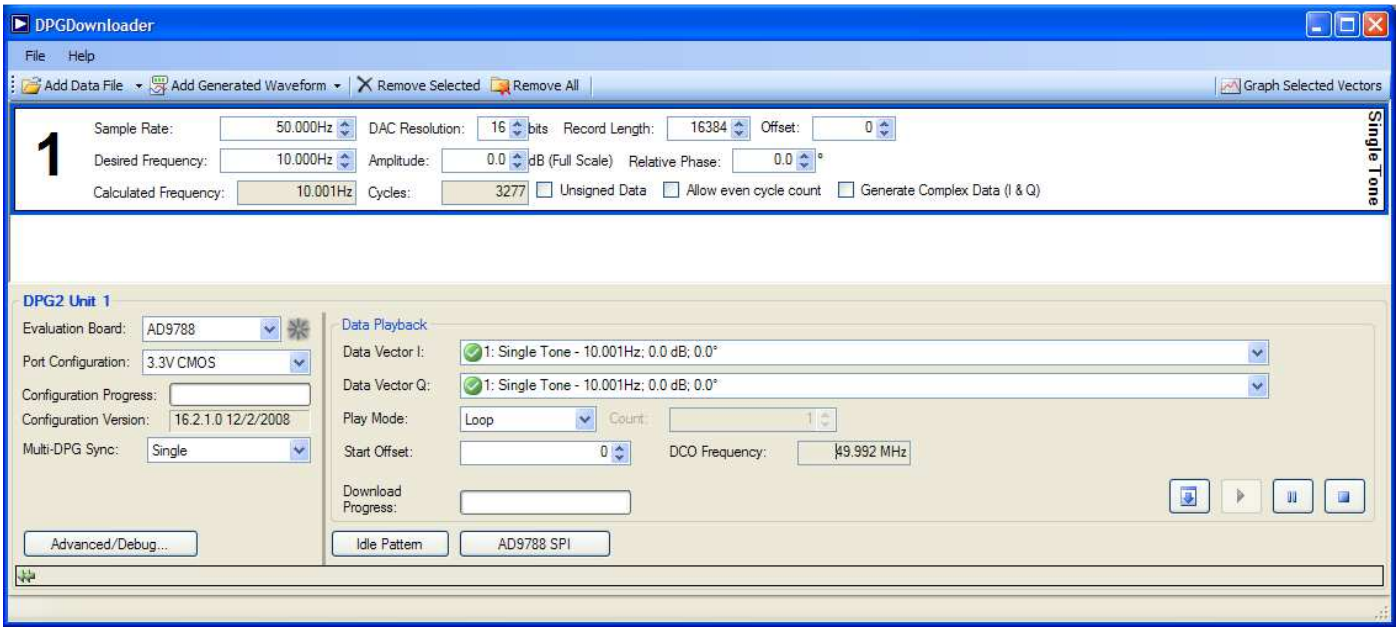


Figure 5 – DPGDownloader Window

- If the AD978*x* evaluation board has been recognized by the PC, AD978*x* should be populated in the Evaluation Board field in the Hardware Config panel.
- Generate a sine wave by pulling down the "Add Generated Waveform" menu and choosing "Single Tone". Fill in the form as shown in (Sample Rate = 50MHz, Desired Frequency = 10 MHz, etc.). Check the "Generate Complex Data (I&Q)" box. Note that the Sample Rate should match the input sample rate and not the DAC update rate. Also, the Unsigned data needs to be unchecked because the AD9788 SPI defaults to 2's complement data format.
- Select the I and Q data vectors in the data selection panel.
- The port configuration will need to be selected 3.3v CMOS the first time you use the AD9779A evaluation board. After the configuration has loaded, the AD9788 SPI box should turn from gray to black.
- Launch the AD9788 SPI GUI by clicking the AD9788 SPI button. Got to the "Data Clock" section and change the Interpolation field to "4x". Select filter mode 0 which is baseband

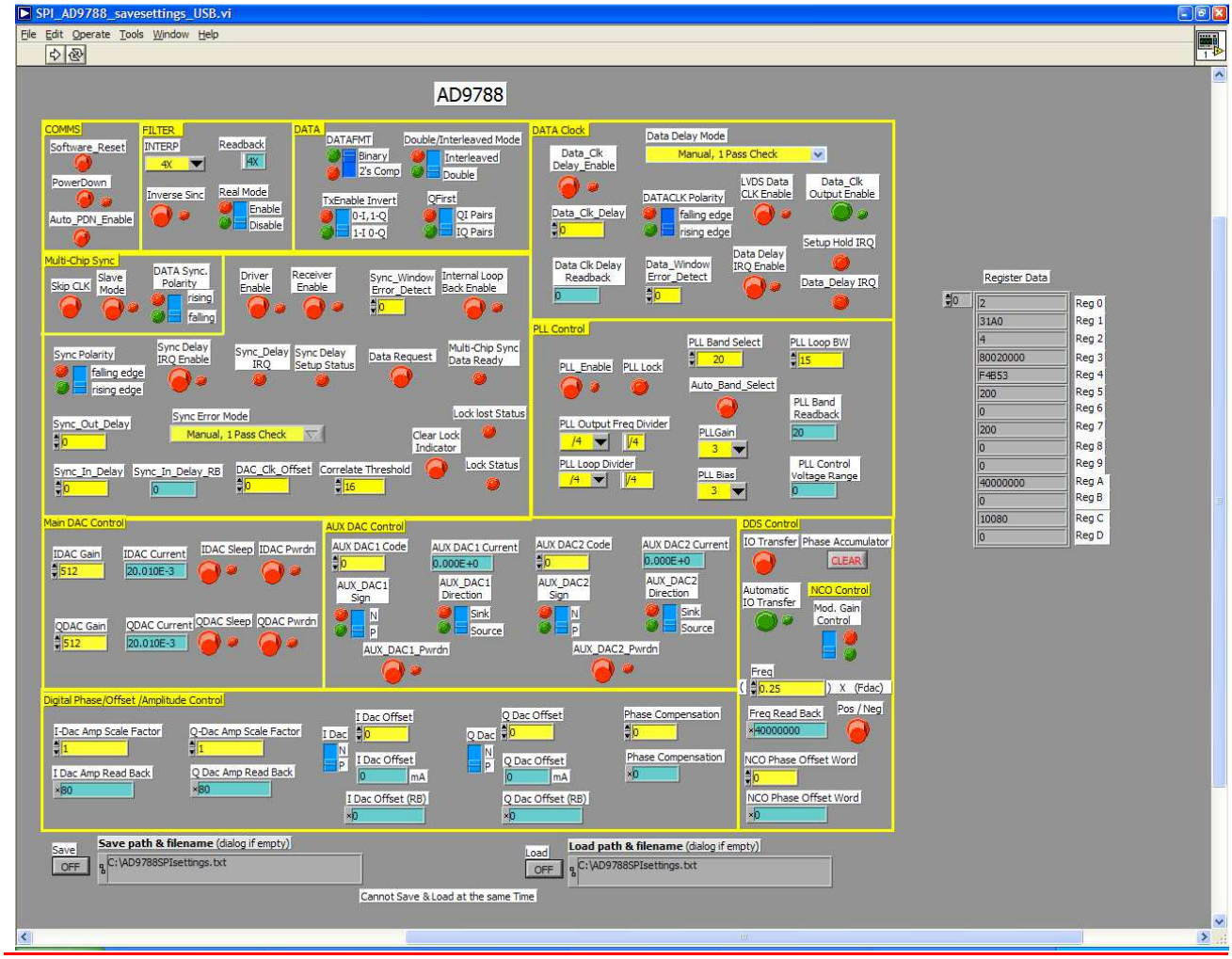


Figure 6 AD9788 SPI VI Panel control

- When the *Run* button is clicked, the SPI controller will run once. It will both write and read from the AD9788. The *Run Forever* control will setup the AD9788, and will continue to read from the chip and will update the SPI when any of the controls change.
- The DCO frequency field in the DPGDownloader window should now be reading something close to 200MHz.
- Next hit the download button. This transfers the data from the PC to the DPG memory.
- When the vector has finished downloading, hit the play button. This starts the DPG2 transmitting data to the eval board.
- The output from J8 should be a clean 29MHz tone as shown below:

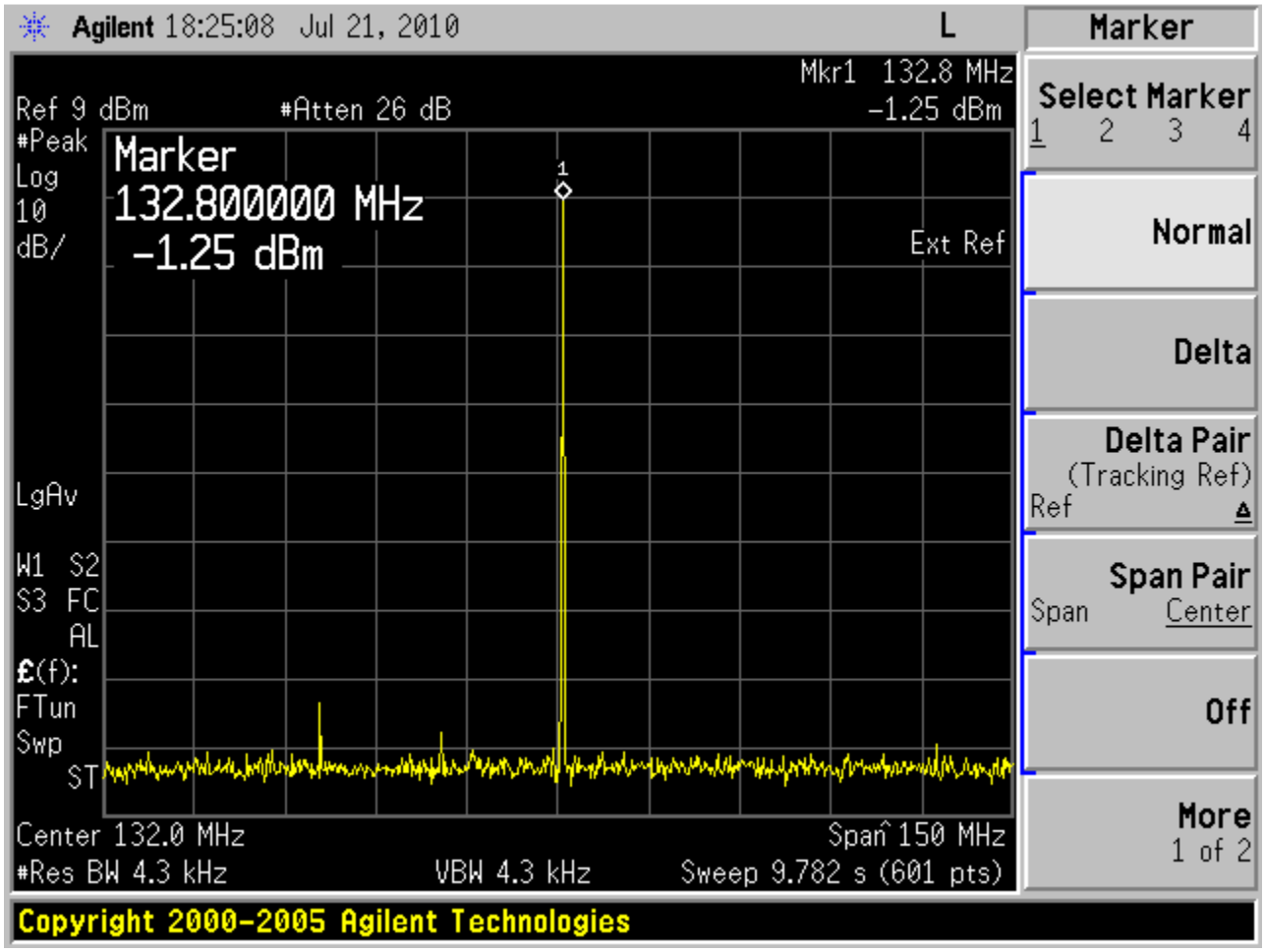


Figure 7 I DAC Output Signal Screenshot

Selecting the Modulator Outputs

By default, solder jumpers JP1, JP2, JP3, and JP4 configure the evaluation board for the DAC outputs to be observed at SMA J4 for IDAC and J8 for QDAC. This jumper setting is shown in 8 a). To connect to the filter that feed ADL5375 the solder jumpers need to be repositioned as shown in 8 b). The output from the ADL5375 Modulator can be observed SMA J6, RF out.

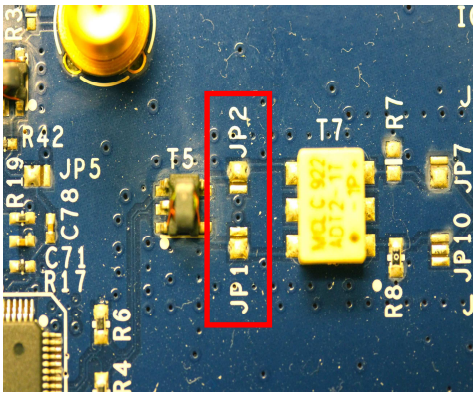
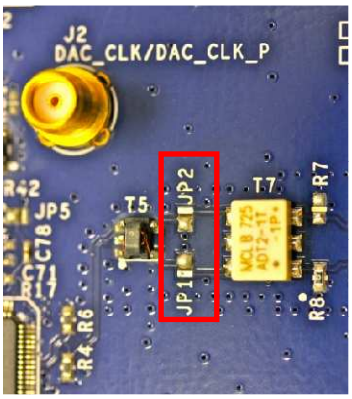


Figure 8 – a) DAC Output Configuration



b) Modulator Output Configuration

AD9788 SPI Application

The SPI application is split into several sections. These sections control the different features of the AD9788 but can be left in the default positions if you are not using the features i.e. internal PLL, multi chip sync, aux DACs . Several of the functions provided by the SPI application are described here, as they relate to the evaluation board. For complete descriptions of each register, refer to the AD9788 datasheet. In the interest of continuous quality improvements, the images below may not exactly match your version of the software. In order to set the registers with the VI you must click the mouse on the arrow under the edit for updating what is selected below or the right circular arrows continuously updates as features are selected in the various sections of the VI

Comms

The COMMS section, is the section in the top left hand corner and has the software reset, power down and auto powerdown enable controls.

Filter

The FILTER section just to the right of the COMMs section provides control over the Interpolation Rate (2x,4x,8x or bypass) and Coarse Modulation via selection of the filter mode with read backs for each. This section also includes the zero stuff feature and inverse Sinc feature.

DATA

The *DATAFMT* field selects the number format of the incoming data, between unsigned (Binary) and signed (2's complement), default on DPG2 is binary but can be switched to 2's complement if desired. The *QFirst* control selects which DAC receives data first from the interleaved bus. For use with the DPG2, this should always be set to *IQ Pairs* and the button should be green next to the IQ pairs. Real mode is for turning off the Q path for a real type application instead of the default complex mode. Single/interleaved is for changing to single port and using an interleaved data format. The TX Invert allows inversion of the Tx Enable signal.

DATA Clock

The data clock section includes control for Data clk delay if needed for adjusting the timing on the interface.

PLL Control

The AD9788 has an on-chip PLL. When *PLL_ENABLE* is turned on, the chip will automatically select the appropriate band using the Divder1 and Divider0 values. The VCO Frequency must be between 1 and 2 GHz for proper operation. The auto-band select can be bypassed by enabling *PLL MANUAL* and entering a band in PLL Band Select. Divider1 and Divider0 must still be chosen appropriately in this mode of operation.

Main DAC Control

This section controls the two main DACs in the AD9788. The Full-Scale Current of each DAC can be set with the *I DAC Gain* and *Q DAC Gain* controls. The 512 default is for 20ma outputs. The *I Sleep* and *Q Sleep* controls put their respective DAC into a low-power sleep state. The IDAC and QDAC power down shuts off the DACs and the signal processing circuit also.

Aux DAC Control

The Aux DAC control section is used to program aux DACs for LO and image suppression out the output of the AQM. The default is the Aux DACs are programmed power down.

SPI Settings Save/load

This section is for saving and reloading your SPI settings so you can use your previous set up. To save a set up slide the save button to turn on and hit the run arrow at the top. To load a file click on the box for browse or type in the file location and click the button to turn on and then hit the run arrow to load this file.

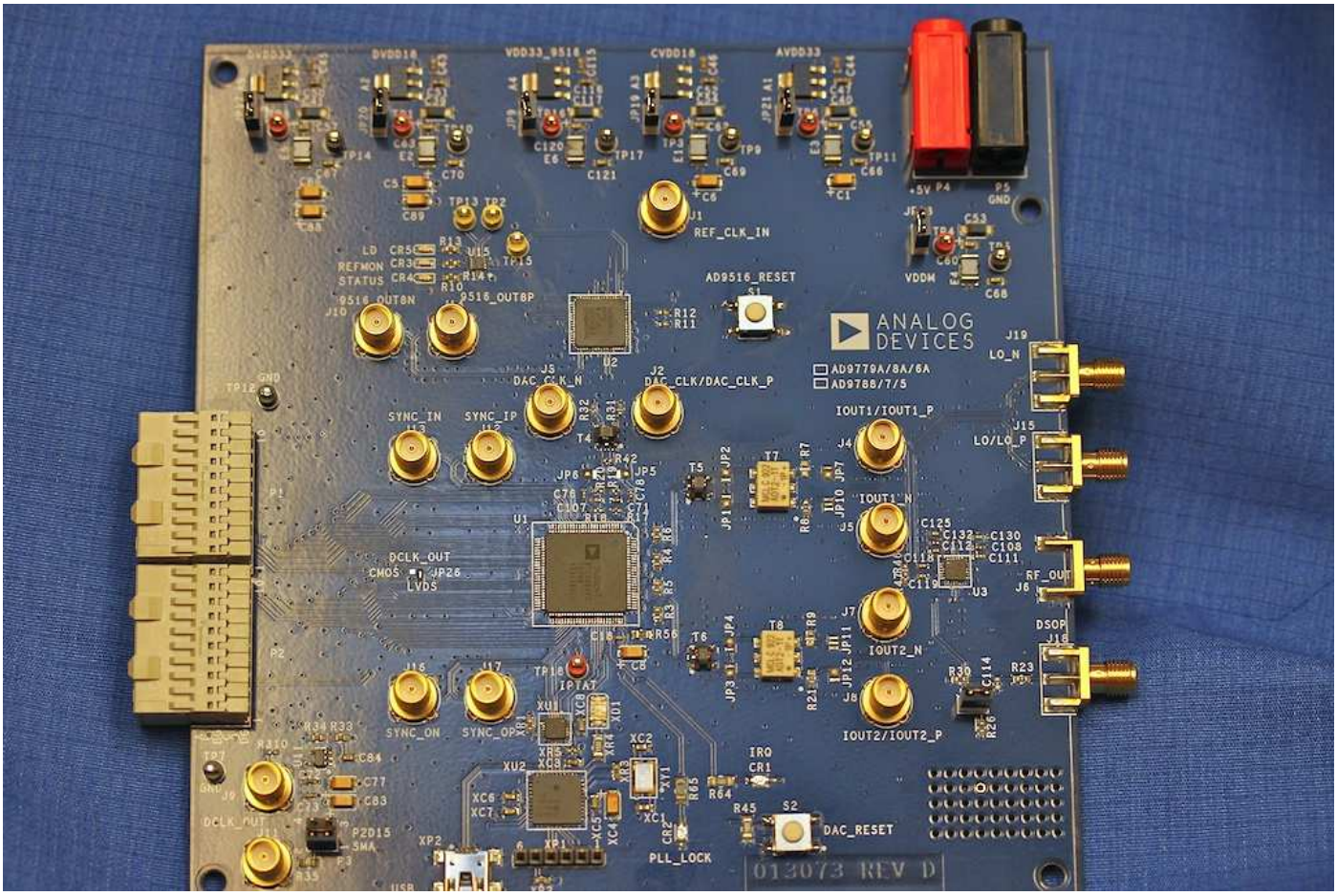


Figure 9 AD9788 Evaluation Board

Using the AD9516

The AD9516 is included so you can test the performance i.e. ACLR with the AD9516 clock multiplication. In order to drive the DAC Clock from AD9516 the jumper J5 and J6 needs to be changed shown in figure 10 a and 10 b. You also need to start up the AD9516 SPI VI that is included in the CD software. First type in your Ref frequency, example in Figure 11 is 122.88 MHz. The Prescaler "P", A and B counters need to be adjusted until you get a Vco Frequency in the range 2.3 to 2.65MHz. The Ref freq will be multiplied by (P*B+A), in this example we used 20

P=8 labeled "divide by 8", B=2, A=4 which yield VCO of 2.4576GHz. We actually want the DAC clock, which will be connected to the PECL output, to be at 4x the reference clock. The VCO divide ratio of 5 along with channel divider bypassed (multiplies by 10 which yields 491.52MHz). There is also an auxiliary output which comes out on SMA J10 and J14. In this example the channel divider 4 is set to 2 which divides the freq by 2 to 245.76MHz and is LVDS type outputs.

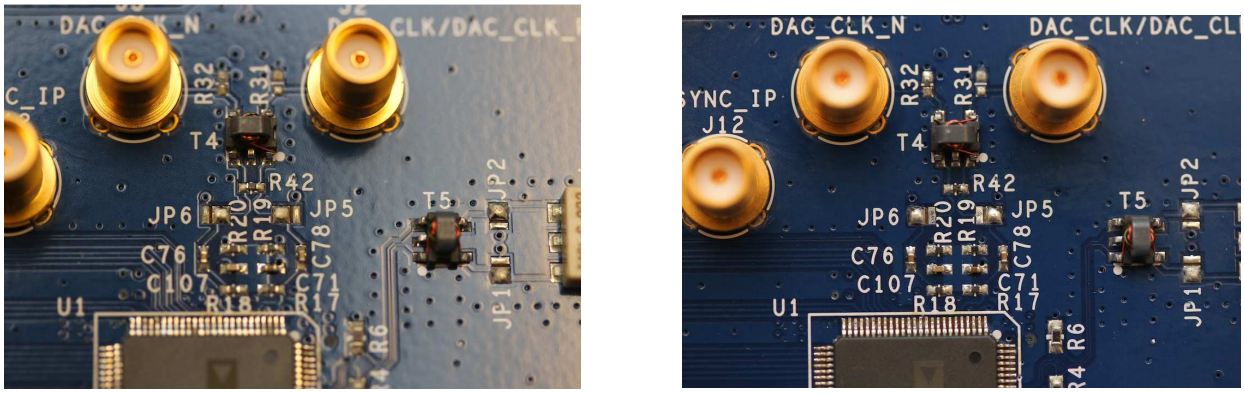


Figure 10 – a) DAC CLK Input configuration b) AD9516 driving DAC CLK Pins

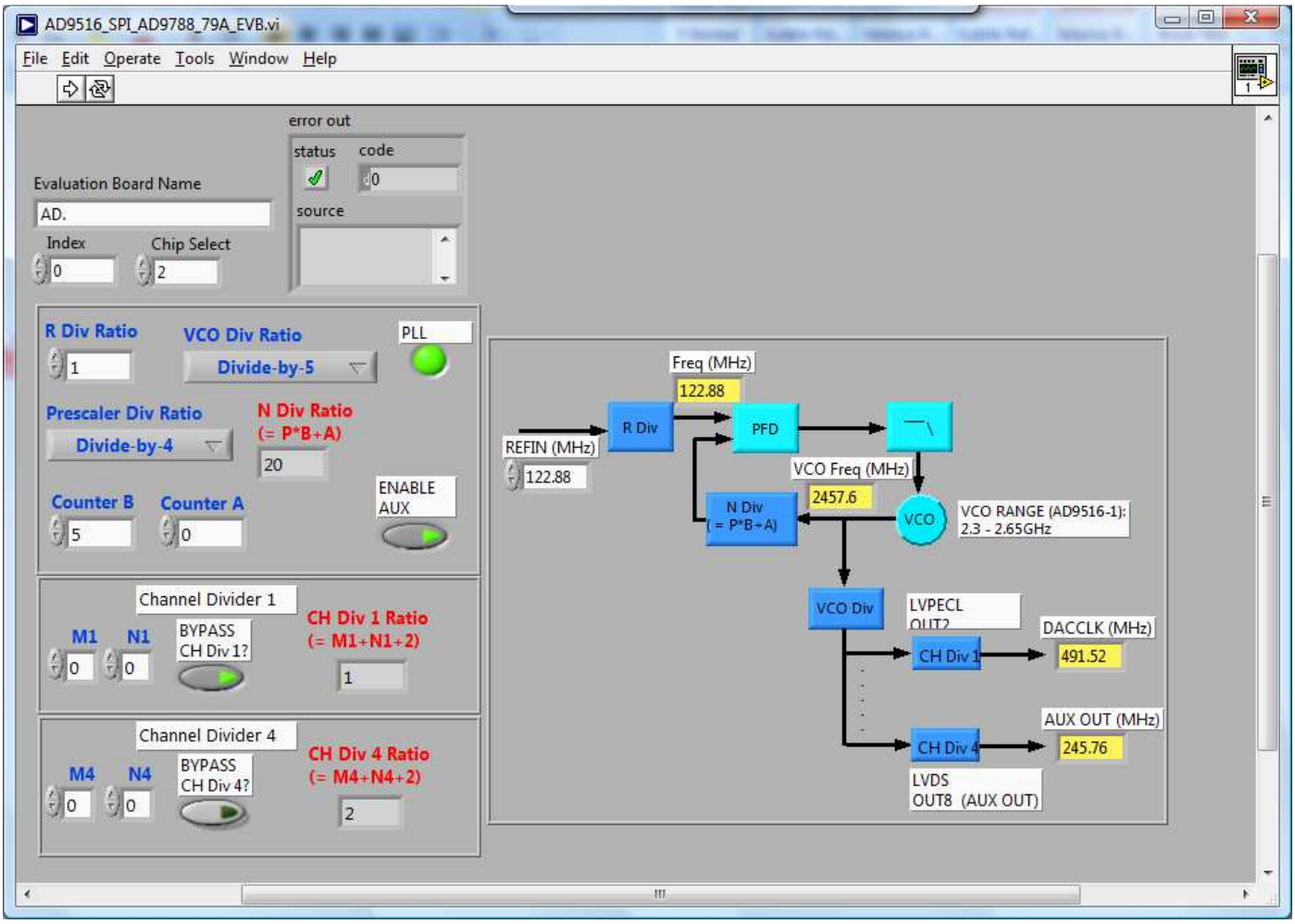


Figure 11 AD9516 SPI Control

Appendix A – DPGDownloader Notes

Detailed documentation for the DPGDownloader Software and the Full DPG Suite can be accessed thru the Help Pull-down menu. Also available from the Help pull-down menu is a shortcut for checking to see if there is a more recent DPGDownloader version available with an option to automatically update the software.

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